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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,828	03/15/2004	Chien-Ting Lai		3134

25859 7590 11/30/2004

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EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/801,828	LAI ET AL.	
	Examiner	Art Unit	
	Theresa T Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-12 and 21 in the reply filed on 10/20/04 is acknowledged.

Drawings

2. Figure 14 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 and 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiramatsu et al. (U.S. Pat. 5,311,040).

Regarding claims 1, 3-4 and 8, Hiramatsu (figure 1) discloses a thin film transistor, comprising:

a substrate (1,3);

a gate electrode 2 is made of Ta or MoTa wherein disposed in the substrate (column 3, lines 25-26);

a gate silicon nitride insulation layer 4 disposed on the substrate and gate electrode (column 3, lines 30-32);

a channel layer 5 disposed on the gate insulation layer 4;

a source/drain ohmic contact layer 8 (column 3, lines 46-47) arranged on the channel layer and at the end of the channel layer;

a source electrode 9 disposed on the substrate and source ohmic contact layer (column 3, lines 46-49);

a drain electrode 10 disposed on the substrate and drain ohmic contact layer (column 3, lines 46-50).

Regarding claims 2 and 5, Hiramatsu (figure 1) discloses the surface of the gate electrode 2 is parallel with the surface of the substrate 3 wherein the cross-section of the gate electrode 2 is trapezoid.

Regarding claim 7, Hiramatsu (figure 1) discloses the substrate 3 is made of silicon oxide (column 3, line 28).

Regarding claims 9-10, Hiramatsu (figure 1) discloses the channel layer 5 is made of amorphous silicon, wherein the source and drain ohmic layers 8 are formed by doping the channel layer 6 (column 3, lines 33-35).

Regarding claim 11, Hiramatsu (figure 1) discloses a display device including a plurality of thin film transistor used to control and drive display material (column 1, lines 13-24), wherein the thin film transistor comprising:

a substrate (1,3);

a gate electrode 2 disposed in the substrate (column 3, lines 25-26);

a gate insulation layer 4 disposed on the substrate and gate electrode (column 3, lines 30-32);

a channel layer 5 disposed on the gate insulation layer 4;

a source/drain ohmic contact layer 8 (column 3, lines 46-47) arranged on the two sides of the channel layer;

a source electrode 9 disposed on the substrate and source ohmic contact layer (column 3, lines 46-49);

a drain electrode 10 disposed on the substrate and drain ohmic contact layer (column 3, lines 46-50).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiramatsu et al. (U.S. Pat. 5,311,040) in view of Vu et al. (U.S. Pat. 5,702,963).

Regarding claim 21, Hiramatsu (figure 1) discloses a thin film transistor comprising:

a substrate (1,3);

a gate electrode 2 disposed in the substrate (column 3, lines 25-26);

a gate insulation layer 4 applied upon the substrate covering both the substrate and the gate electrode (column 3, lines 30-32);

a channel layer 5 applied upon the gate insulation layer 4 and only covering a central portion of an upper face of the gate insulation layer;

a source electrode 9 disposed upon one side of the channel layer 5 and further covering a portion of the gate insulation layer 4 wherein the portion is exposed to an exterior before the source electrode is applied thereto; and

a drain electrode 10 disposed upon the other side of the channel layer 5 and further covering another portion of the gate insulation layer 4 wherein the another portion is exposed to the exterior before the drain electrode is applied thereto. It is noted that the process limitation (exposed before) would not carry patentable weight in this

claim drawn to a structure, because distinct structure is not necessarily produced. In re Thorpe, 227 USPQ 964 (Fed. Cir. 1985).

Hiramatsu does not disclose a substrate defining a cavity in an upper face and a gate electrode filled in the cavity. However, Vu (figures 15D-15E) teaches a substrate 1054 defining a cavity 1062 in an upper face and a gate electrode filled in the cavity. Accordingly, it would have been obvious to form the gate electrode of Hiramatsu by defining a cavity in the substrate because such forming cavity would permit the forming of the gate electrode in a backside region of the substrate, as taught by Vu (column 3, lines 54-60).

Regarding claim 6, as discussed in claim 1 above, Hiramatsu does not disclose the cross-section of the gate electrode is rectangle. However, Vu (in figures 15D-15E) teaches the cross-section of the gate electrode is rectangle. It would have been obvious to form the cross-section of the gate electrode is rectangle in Hiramatsu's structure, because the shapes of gate electrode are not critical, it can be optimized depending upon the resistance which is desired for gate electrode.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TD
November 19, 2004.

PHAT X. CAO
PRIMARY EXAMINER